OBJECTIVES: At the end of this section, the student will be able to do the following:

- Describe Manufacturing Test Flow.
- Discuss Windowed user interface and Command Line Test Executive versions of the Modular Test Architecture (MTA) Diagnostics
- Explain schematic layouts, signal tracing, & component location.
Manufacturing Test Flow
ATE = Automatic Test Equipment
STBL = System Test Board Level
SST = Simplified Systems Test
ESS = Environmental Stress Test
EST = Extended System Test
PEST = Post EST
FINAL ASSY
SHIP
ATE TEST STEP

• Uses HP and GENRAD based ICT testers
• Run at nominal speed - 6 MHz
  • 12 MHz & 20MHz options available
• Voltage margined (+6%)
• Vacuum fixture based interface to UUT
  – Can also be used at post-IR oven board assembly (prior to wave solder) if fixture has overclamp
• Tests performed
  – Fixture and board shorts & opens
  – Analog components function and opens
  – Clock frequencies
  – Digital components function & opens
STBL TEST STEP

• Full speed system test run at board level
  – Optional voltage margining (Nominal and +/- 5%)
  – Automated test selection, CMOS/ICU/EISA/ESCD setting, and Flash BIOS update

• ASTF (At Speed Test Fixture) hardware used for test environment
  – Monitor, Keyboard, Mouse, Floppy (A & B), Hard Disks (IDE & SCSI), Loopbacks, Network board, EISA test board, PCI Video, ISA or PCI LAN Board, Test Hook Board, Control Panel, Power Supply
  – Comes in 3 flavors of interfaces to UUT: Removable Vacuum Fixture (CRV), Manual Connection Platform (CRP), or Xtended Xpress Platform (CRX).

• Test routines served from central NT Based test server
  – Network connection via embedded network add-in board
  – DOS based test routines written in Microsoft C / ASM
  – Common code base at STBL, SST, and EST
STBL PROCESS FLOW

FINAL ASSY

Ethernet

Test Server

Factory Information System (IFICS)

Production Board Test (STBL)

ATE

pass

fail

Rework

Debug

pass

fail

ESS/OQA/PKG/SHIP
Modular Test Architecture (MTA) Diagnostics
Modular Test Architecture (MTA) Diagnostics

- The MTA Diagnostics are typically used by technicians to debug problems after the board has booted an operating system.
  - Examples are Serial, Parallel, Video, and Sound tests.
  - Also, many MTA diagnostics will find problems that were not detected by the BIOS during POST.
    - e.g.- Memory patterns tests such as data ripple, checkerboard patterns, sliding ones, & random patterns
- MTA is covered here to familiarize technicians with the available features of these diagnostics.

- The focus of this course is on the system board components that contribute to pre-boot failures.
  - Pre-boot problems are usually found during the Power On Self Test (POST).
Modular Test Architecture (MTA) Diagnostics

OVERVIEW

- Used in Intel factories for over 5 years
- Available as Intel product
- Used at many Intel customers for system integration and field repair
- Code written in Microsoft C and ASM
- Runs under DOS
- Modular and configurable
- Tests all major system components
- Command line or windowed human interface
Modular Test Architecture (MTA) Diagnostics

**Correlation / Commonality**

Same MTA Test Architecture For All Full Speed Functional Tests

**ATE**
In-Circuit Test

**Functional Board Test**

**System Assembly**

**System Level Test**

MTA Diagnostics for Audits, Incoming, Repair, Field, and Customer Test

MTA = Modular Test Architecture
ATE = Automatic Test Equipment
STBL = Systems Test Board Level

SST = Single Step Test
EST = Extended Systems Tests

PC Architecture For Technicians Level-1
Technical Excellence Development Series

Rev. 1.0 Sys MFG T/ED
4/25/2003

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Modular Test Architecture (MTA) Diagnostics

TEST SOLUTIONS FOR EVERYONE

DESIGN ENGINEERING TESTS
COMPATIBILITY TESTS
ENVIRONMENTAL TESTS
RELIABILITY TESTS
INCOMING INSPECTION TESTS
FACTORY BOARD TESTS
FACTORY SYSTEM TESTS
FACTORY AUDIT TESTS
FACTORY PROCESS TOOLS
REPAIR CENTER TESTS
CUSTOMER DIAGNOSTICS
Two interfaces exist for the MTA tests.

- `T (t.exe)` is the *command line* interface for the tests,
- *Testview* is a menu *(GUI)* interface.
- Both interfaces allow users to run test sequences through a numerical mapping.
- In both cases a PKG file is used to map names and numbers to a test invocation line.
Modular Test Architecture (MTA) Diagnostics

- **Manufacturing Version:**
  - This is a **Test executive** based MTA Diagnostics package structured as a batch file.
  - **T (t.exe)** is used to run tests from the DOS command line or the batch file.
  - It is tailored specifically for a particular test step in the Intel manufacturing process.
  - It uses the PASSFAIL module to indicate to the user at the end of the test run whether the board or system passed or failed by displaying a red or green screen.
  - There are separate packages for STBL and SST/EST test steps. **Typically used for all in-line automated test steps.**
Modular Test Architecture (MTA) Diagnostics

Command Line Test Executive

- Referred to as “T” (T.EXE)
- Uses test suite structure defined by the .PKG files.
  - Defaults to T.PKG unless /PKG parameter specified on command line. Example: \t /pkg my.pkg
- Use /DT command line flag to display available test modules and subtests with logical sequence numbers assigned to each of them.
- Typically used in automated manufacturing environment where human interaction is minimized
Modular Test Architecture (MTA) Diagnostics

Command Line Test Executive

T invocation syntax: T <run_list> <cmd_flag_list>

T Run all enabled subtests in all modules in the PKG file.
T FLOPPY Run all enabled subtests in the FLOPPY module.
T 1.1 Run the first subtest of the first module in the PKG file, if enabled.
T FLOPPY.1 Run the first subtest of the FLOPPY module, if enabled.
T 1.3-1.7 Run subtests 3 through 7 that are enabled of the first module in the PKG file.
T {1,5,7} Run all enabled subtests in modules 1, 5, and 7.
Modular Test Architecture (MTA) Diagnostics

Field Version: (GUI)

- The Field Version is used for off-line interactive debug
- This is the **Testview** test executive based MTA Diagnostics package.
  - This uses the Testview windowed interface tailored for the human interactive user.
  - It provides the greatest on-line test configurability.
- **Typically used for board and system debug.**
  - INTELPCDIAG is a field version.
Modular Test Architecture (MTA) Diagnostics

Testview Test Executive

• Windowed user interface

• Allows control of what tests are run and how configured

• Load and save custom test suite (.PKG) configurations

• Context sensitive help

• Reminder of interactive, hardware required, and destructive tests when user enables each test

• Sign-on line of windowed menu screen, colors, default .PKG file, and command line parameters can be customized through Testview.ini file
### Modular Test Architecture (MTA) Diagnostics

#### Testview Test Test Executive (GUI)

**Windowed Screen Example**

<table>
<thead>
<tr>
<th>TEST</th>
<th>ERRORS</th>
<th>SUMMARY</th>
<th>CONFIGURATION</th>
<th>OPTIONS</th>
<th>HELP</th>
<th>QUIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>POST</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>KB</td>
<td>1</td>
<td>CPU_TYPE</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIDEO</td>
<td>2</td>
<td>FLOATING_POINT_UNIT</td>
<td>3</td>
<td>CLOCK_SPEED</td>
<td>4</td>
<td>CPU_STEPPI NG</td>
</tr>
<tr>
<td>MOUSE</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RTC</td>
<td>5</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>PIC</td>
<td>6</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>PIT</td>
<td>7</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>DMA</td>
<td>8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PARALLEL</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>COM1</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>COM2</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LAN</td>
<td>12</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HARD_DISK_0</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HARD_DISK_1</td>
<td>14</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FLOPPY_A</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DMA</td>
<td>16</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<ENTER> display sub-menu  <ESCAPE> exit TESTVIEW <F1> help <F2> run module  [TAB]
Modular Test Architecture (MTA) Diagnostics

Example Test Modules

- **CPU** -- CPU identification tests. Checks CPU type, CPU clock speed (with/without cache), CPU stepping, and floating point unit presence to determine that the correct CPU is installed in the board and the clock frequency is set correctly.

- **DMA** -- Direct memory access controller tests. Checks page registers, address registers, count registers, DOS transfers, and scratch transfers.

- **FLOPPY** -- Floppy controller and floppy drive test. Checks reset command, status, disk type, get FDD params, set FDD params, format track, verify track, disk format, disk verify, floppy write, floppy read, random seek, disk change, sequential write / read, funnel seek, and write / read limits. Supports 3-mode floppies.

- **MSDRAM** -- System memory and memory controller tests. Tests up to 4GB. Checks refresh request, address patterns, address ripple, data ripple, checkerboard patterns, sliding ones, random patterns, cache random patterns, cache checkerboard, cache address patterns, cache sliding ones, cache pseudo-random patterns, ...
Modular Test Architecture (MTA) Diagnostics

Example Test Modules

- **PARIO** -- Parallel I/O port tests. Checks presence, data port, control port, external loopback, and interrupts. Supports configurable port locations and loopback wiring.

- **PCI** -- PCI BIOS and device presence tests. Checks if a BIOS that supports PCI is present. Checks to see that the right PCI devices are present on the appropriate PCI buses (vendor-id, device_id, bus, device_number, function_number). Also has a display function to display all PCI devices.

- **SERIO** -- Serial controller tests. Checks port presence, internal data bus, modem status registers, baud rates (110 to 57.6KB), word length, stop bits, parity, interrupt, external data bus, external modem status register, BIOS INT 0x14 functions, and FIFO.

- **SND_4232** -- Crystal Semiconductor 4232 audio controller tests. Checks Windows sound system registers, internal FM loopback, external FM-CD loopback, internal line loopback, external line loopback, external microphone loopback, joystick loopback, MIDI loopback, FM interrupts, MIDI interrupts, CS4232 interrupt, play CD sample, display Plug and Play resources utility.
Modular Test Architecture (MTA) Diagnostics

- Execution of a test is controlled through the run time flags. These flags are passed to the test when it is spawned by Testview.

- `/DT [nn] - Display tests`. Lists the names and numbers of all subtests in the PKG file with a "+" or "-" for each subtest indicating it is enabled.

- `/N nn - Number of loops`. This flag indicates the number of complete passes to be taken through the run-list. Zero (0) indicates run forever.

- `/HE - Halt on error`. Causes testing to halt when an error occurs.
EXAMPLE ALGORITHM

- Found in HELP file for each test. (e.g. - DMA.HLP)

- The 8 DMA Address Registers are tested for address uniqueness by writing a 0 through 7 pattern into the low byte and an inverse pattern in the high byte of each register so that each register contains a unique value. The results are then checked and if an error is detected an error message is displayed.

- The 8 DMA Address Registers are then tested for data integrity by writing the low byte with a data pattern of 00 through FF and the high byte with the inverse pattern. The Address Registers are then checked for the proper result. The low byte is then written with an inverse pattern and the high byte written with a 00 through FF pattern. For each increment of the data the Address Registers are read and checked for proper result. An error message is displayed if a miscompare is detected.
Module Test Architecture (MTA) Diagnostics

**EXAMPLE ERROR MESSAGE:**

- Found in HELP file for each test. (e.g. - VID_ATI.HLP)
- ***ERROR VID_ATI.CNTRL_REG
- At Address = [XXXX], Expected Data = [XX], Received Data = [XX]
- Standard Error Code = 02B02000
- Standard Error Code = 02B02001

**DEBUG HINTS**

- Check the bi-directional data buffers that controls the data in/out to Video Controller.
- Check the memory clock(MCLOCK), video clock(VLOCK) I/O R/W.
- Check the strapping resistors to see if they are configured for Intel(R) Local Bus.

**NOTE:** (***) imbedded in help file.
Intel Schematics
Intel Schematics:

- Overall layout of schematics:
- Signal tracing:
- Locating components:
Schematics - Layout

Typically, each sheet of the schematics is individually numbered, from 1 to the last page.

- **The First Sheet:**
  - Shows general Notes and the power distribution to various ICs.

- **The Next Sheet(s):**
  - Presents overall block diagram of product with functional regions sectioned off.
  - Each section is expanded upon in separate sections of the schematic.
  - Indicates major busses interconnecting regions
Schematics - Layout

At the beginning of each section:

- A more detailed block diagram of the section showing major components.
- Bus interconnections are shown in much greater detail.
- Pages within each section have an additional Section Page number, e.g. C1, C2 etc.

Individual sheets:

- Show each and every IC, resistor, capacitor, etc.
- Signal names from point to point on the schematic.
Schematics- Tracing signals

Signal Names:

- Signal names are assigned to all lines interconnecting components.
- Signal names are often the signal names used on the major ICs
  - (e.g. - BRDY#, FRAME-, BIOSCS*, NMI, SD07, ).
- Each name indicates Active logic level:
- Active suggests when the signal is performing its intended job.
  - e.g. CE = Chip Enable
- Active-when-logical-high, or Active High signals are the default case.
  - e.g. When CE = 1 then the Chip is Enabled
Schematics- Tracing signals

Two frequently used methods to indicate Active Low signals are:

- Minus sign  e.g. CE-
- Hash sign   e.g. CE#
- Asterisk    e.g. CE*
- Underscore  e.g. CE_
- Slash       e.g. /CE

Bus signals are numbered such that the highest number is the most significant (e.g. A31:0)

- A31 is the most significant address line
- A0 the least significant address line.
Schematics- Tracing signals

Following signals:

- Power supply and ground levels are presumed global to the schematics.
- Each signal leaving any sheet of the schematic has the number of other sheet(s) it goes to.
  - Beware: All sheet number cross-references may not be included on every sheet.
- Exercise: Review the schematics supplied for the features outlined above.
Schematics - Locating Component

Board construction:
- Typically the PCB uses 4-layer construction:
- 5 Volt and ground layers are within the sandwich.
- Upper and lower surfaces of the board are signal layers.
- Signals frequently cross between upper/lower layers through solder Vias.
- Pin 1 is often indicated with: □ or ○

Component type designators:
- ICs have a ‘U’ prefix, transistors ‘Q’, diodes (all types) ‘CR’
- Resistors have ‘R’ prefix, resistor packs ‘RP’, capacitors ‘C’, and inductors ‘L’
The Component Grid

- Grid lettering is printed along the board edge dividing the board into approx. 1 inch squares.
- Letters A, B, C... are on one axis, the numbers 1, 2, 3 along the other.
- The complete component legend combines designator and grid location:
  - e.g. U5F3, the third IC in grid location 5F (See Diagram).

Exercise: Locate the sample components requested by the instructor.
Schematics- Locating Component

Circuit Board Grid Location System (e.g. U5F3):

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
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</tbody>
</table>

Circuit Board Outline

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
</table>
SUMMARY
WE HAVE DISCUSSED THE FOLLOWING:

- The Manufacturing Test Flow.
- The Windowed user interface and Command Line Test Executive versions of the Modular Test Architecture (MTA) Diagnostics
- Schematic layouts, signal tracing, & component location.